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DRIFT COMPENSATION SYSTEM AND METHOD IN A CLOCK DEVICE OF AN ELECTRONIC CIRCUIT

Abstract

A drift compensation system includes a first clock phase alignment circuit adapted for providing an output clock signal which is frequency locked to an input reference clock signal; a second clock phase alignment circuit identical to the first clock phase alignment circuit but wherein the reference clock signal is the output clock signal provided by the first clock phase alignment circuit; first deviation means at the output of the first clock phase alignment circuit for providing a first deviation between its current clock phase and its initial clock phase; second deviation means at the output of the second clock phase alignment circuit for providing a second deviation between its current clock phase and its initial clock phase; and a phase control logic adapted for providing first phase shift signals as inputs to the first clock phase alignment circuit in order to cancel the phase shift between the output clock signal and the reference clock signal in response to the difference between the first and the second deviations.